



# PD57030-E PD57030S-E

## RF POWER transistor, LDMOST plastic family N-Channel enhancement-mode lateral MOSFETs

### General features

- Excellent thermal stability
- Common source configuration
- $P_{OUT} = 30W$  with 14dB gain @ 945MHz / 28V
- New RF plastic package

### Description

The PD57030 is a common source N-Channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 28 V in common source mode at frequencies up to 1 GHz.

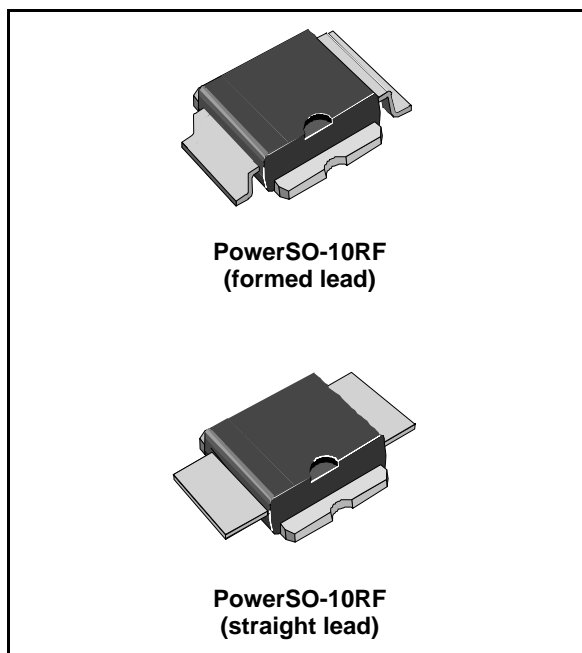
PD57030 boasts the excellent gain, linearity and reliability of ST's latest LDMOS technology mounted in the first true SMD plastic RF power package, PowerSO-10RF. PD57030's superior linearity performance makes it an ideal solution for base station applications.

The PowerSO-10 plastic package, designed to offer high reliability, is the first ST JEDEC approved, high power SMD package. It has been specially optimized for RF needs and offers excellent RF performances and ease of assembly.

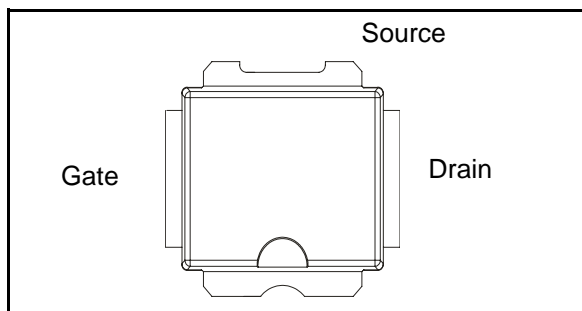
Mounting recommendations are available in [www.st.com/rf/](http://www.st.com/rf/) (look for application note AN1294)

### Order codes

Part number	Package	Packing
PD57030-E	PowerSO-10RF (formed lead)	Tube
PD57030S-E	PowerSO-10RF (straight lead)	Tube
PD57030TR-E	PowerSO-10RF (formed lead)	Tape and reel
PD57030STR-E	PowerSO-10RF (straight lead)	Tape and reel



### Pin connection



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# 1 Electrical data

## 1.1 Maximum ratings

Table 1. Absolute maximum ratings ( $T_{CASE} = 25^{\circ}C$ )

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current	4	A
$P_{DISS}$	Power dissipation (@ $T_C = 70^{\circ}C$ )	52.8	W
$T_J$	Max. operating junction temperature	165	$^{\circ}C$
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$

## 1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction - case thermal resistance	1.8	$^{\circ}C/W$

## 2 Electrical characteristics

$$T_{CASE} = +25\text{ }^{\circ}\text{C}$$

### 2.1 Static

**Table 3. Static**

Symbol	Test conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	$I_{DS} = 10\text{ mA}$	65			V
$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			1	$\mu\text{A}$
$V_{GS(Q)}$	$V_{DS} = 28\text{ V}$	$I_D = 50\text{ mA}$	2.0		5.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$		1.3		V
$g_{FS}$	$V_{DS} = 10\text{ V}$	$I_D = 3\text{ A}$		1.8		mho
$C_{ISS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		57		pF
$C_{OSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		30		pF
$C_{RSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$		2.3		pF

### 2.2 Dynamic

**Table 4. Dynamic**

Symbol	Test conditions		Min	Typ	Max	Unit
$P_{OUT}$	$V_{DS} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $f = 945\text{ MHz}$	30			W
$G_P$	$V_{DS} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $P_{OUT} = 30\text{ W}$ $f = 945\text{ MHz}$	13	14		dB
$\eta_D$	$V_{DS} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $P_{OUT} = 30\text{ W}$ $f = 945\text{ MHz}$	45	53		%
Load mismatch	$V_{DS} = 28\text{ V}$	$I_{DQ} = 50\text{ mA}$ $P_{OUT} = 30\text{ W}$ $f = 945\text{ MHz}$ ALL PHASE ANGLES	10:1			VSWR

### 3 Impedance

Figure 1. Current conventions

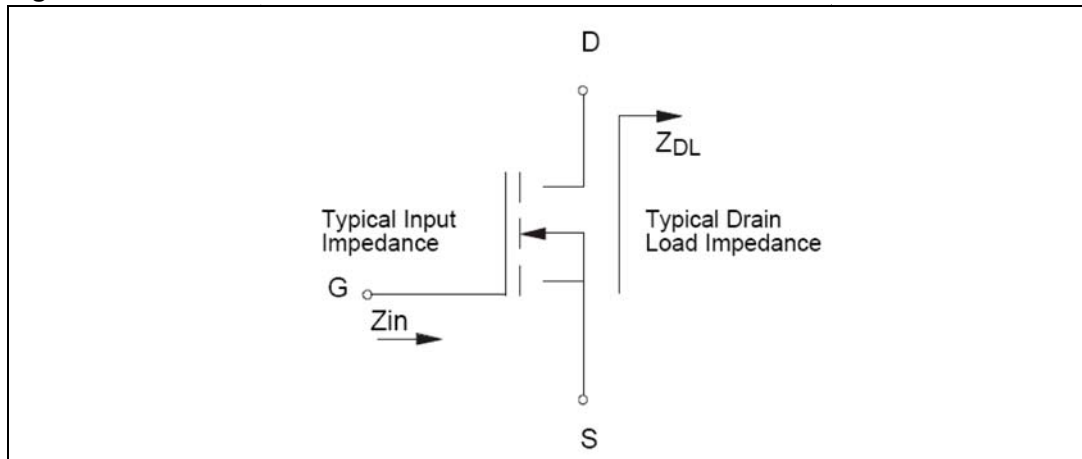
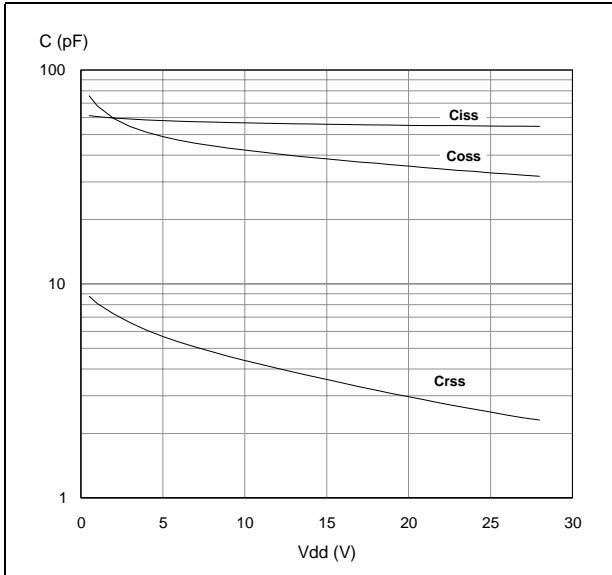


Table 5. Impedance data

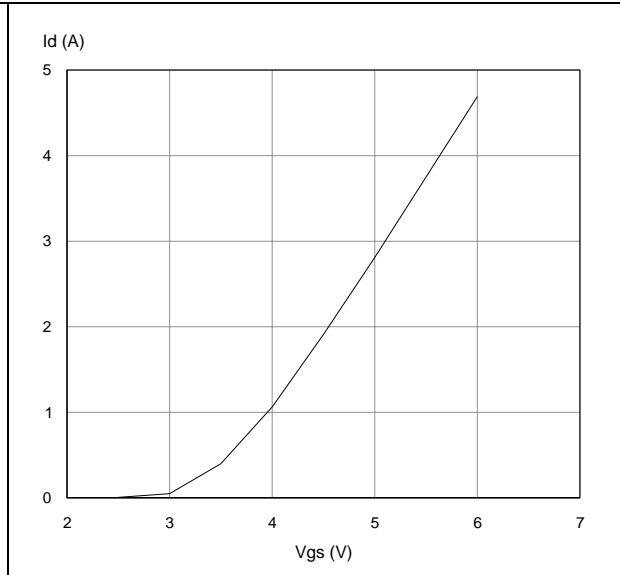
Freq. (MHz)	$Z_{IN}$ ( $\Omega$ )	$Z_{DL}$ ( $\Omega$ )
925	$0.929 - j 0.315$	$2.60 + j 1.45$
945	$0.809 - j 0.085$	$2.46 + j 0.492$
960	$0.763 - j 0.428$	$2.35 + j 0.591$

# 4 Typical performance

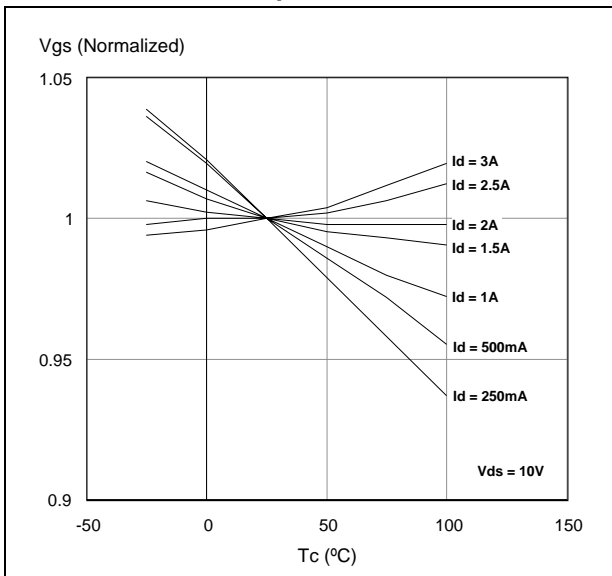
**Figure 2. Capacitance vs supply voltage**



**Figure 3. Drain current vs gate source voltage**



**Figure 4. Gate-source voltage vs case temperature**



PD57030S

Figure 5. Output power vs input power

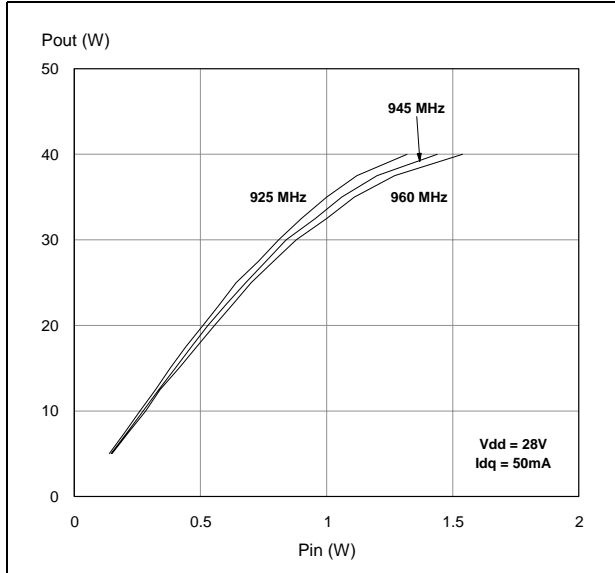


Figure 6. Input return loss vs output power

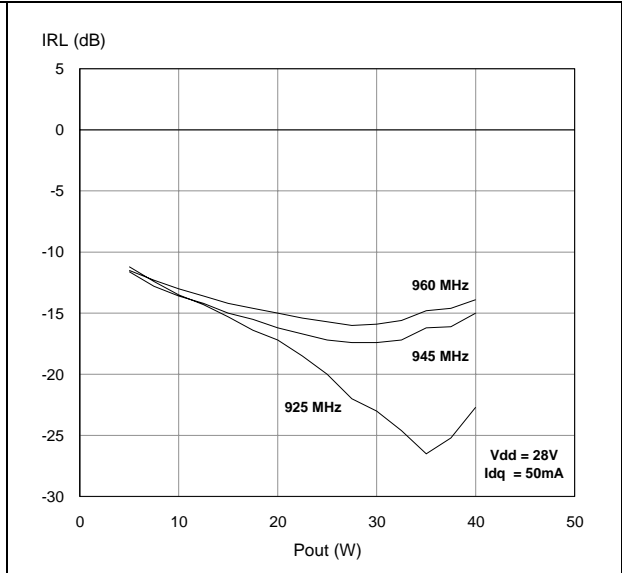


Figure 7. Power gain vs output power

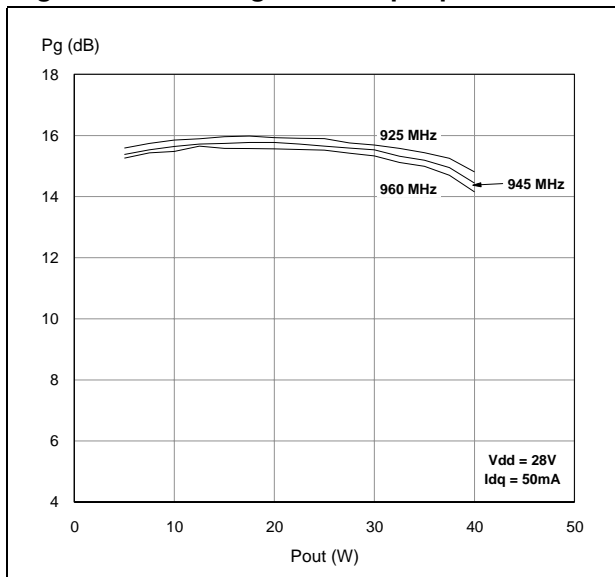


Figure 8. Efficiency vs output power

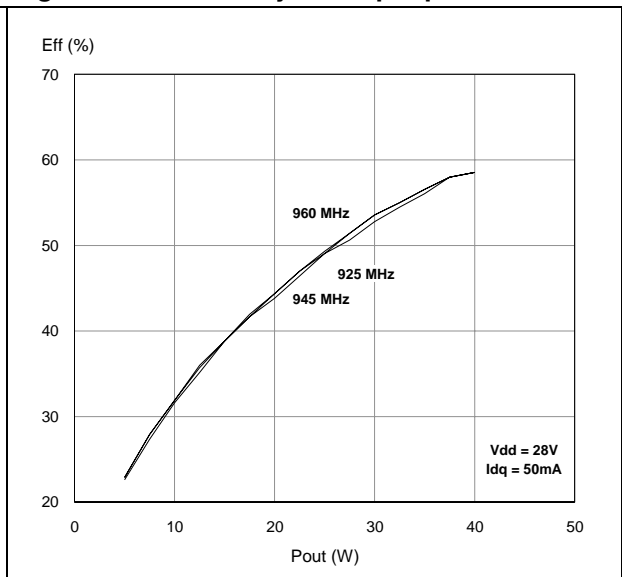


Figure 9. Output power vs bias current

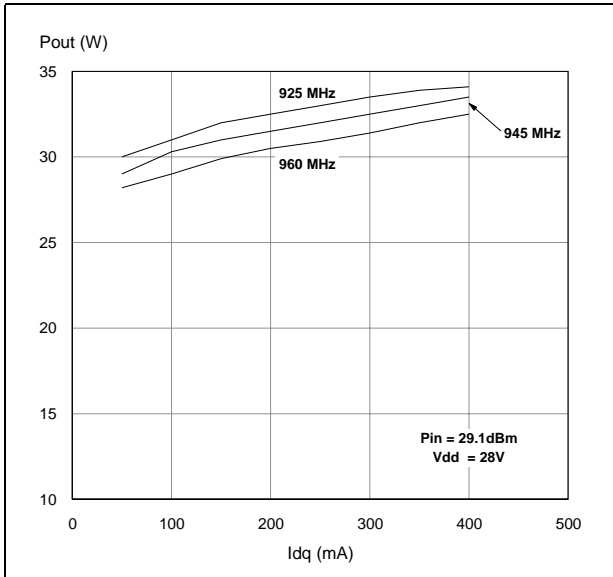


Figure 10. Efficiency vs bias current

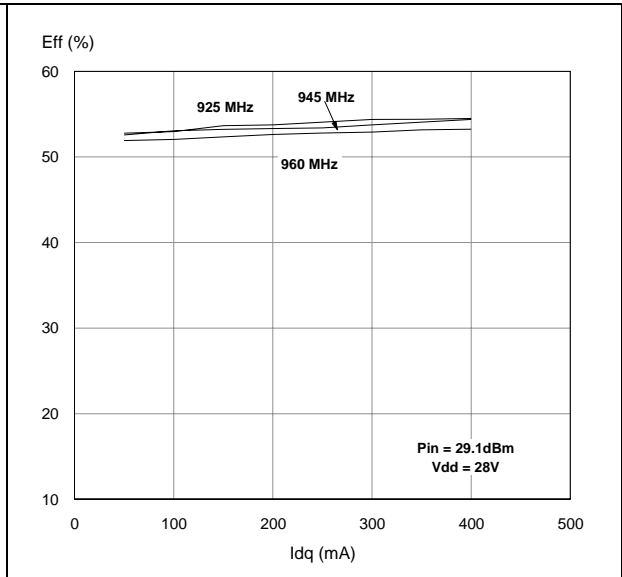


Figure 11. Output power vs drain voltage

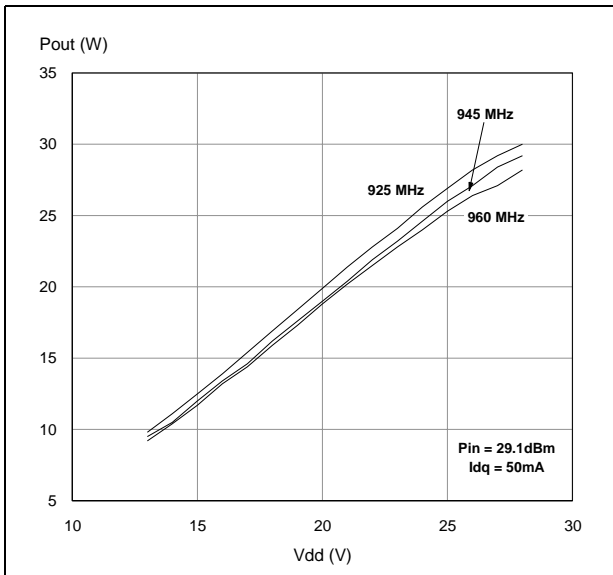


Figure 12. Efficiency vs drain voltage

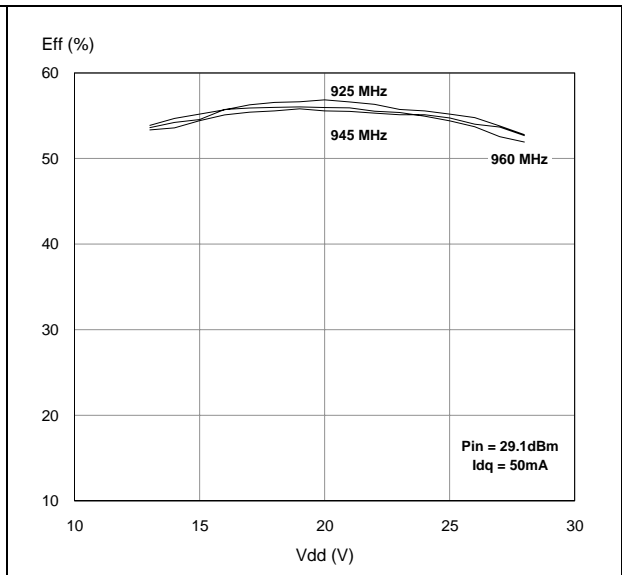
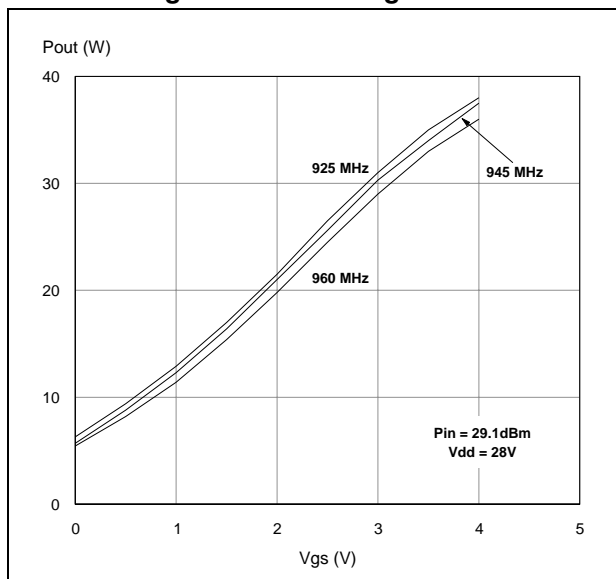




Figure 13. Output power vs gate-source voltage



# 5 Test circuit

Figure 14. Test circuit schematic

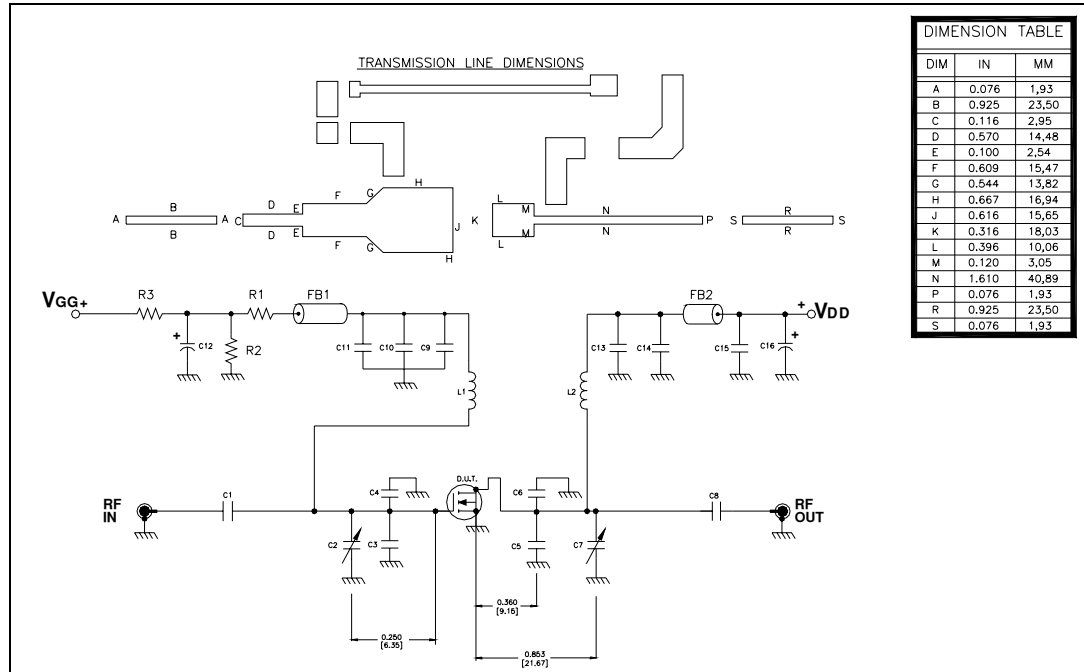


Table 6. Test circuit component part list

Component	Description
C1, C8, C9, C13	47pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C2, C7	0.8-8.0pF GIGA TRIM VARIABLE CAPACITOR
C3, C4, C5, C6	7.5pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C10	1000pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C11, C15	0.1μF / 500V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C12	10μF / 50V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C14	100pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C16	220μF / 63V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
R1	18KΩ 1W SURFACE MOUNT CHIP RESISTOR
R2	4.7MΩ 1W SURFACE MOUNT CHIP RESISTOR
R3	120Ω 2W SURFACE MOUNT CHIP RESISTOR
FB1, FB2	SHIELD BEAD SURFACE MOUNT EMI
L1, L2	INDUCTOR, 5TURNS AIR WOUND #22AWG, ID=0.059[1.49], NYLON COATED MAGNET WIRE

Figure 15. Test circuit photomaster

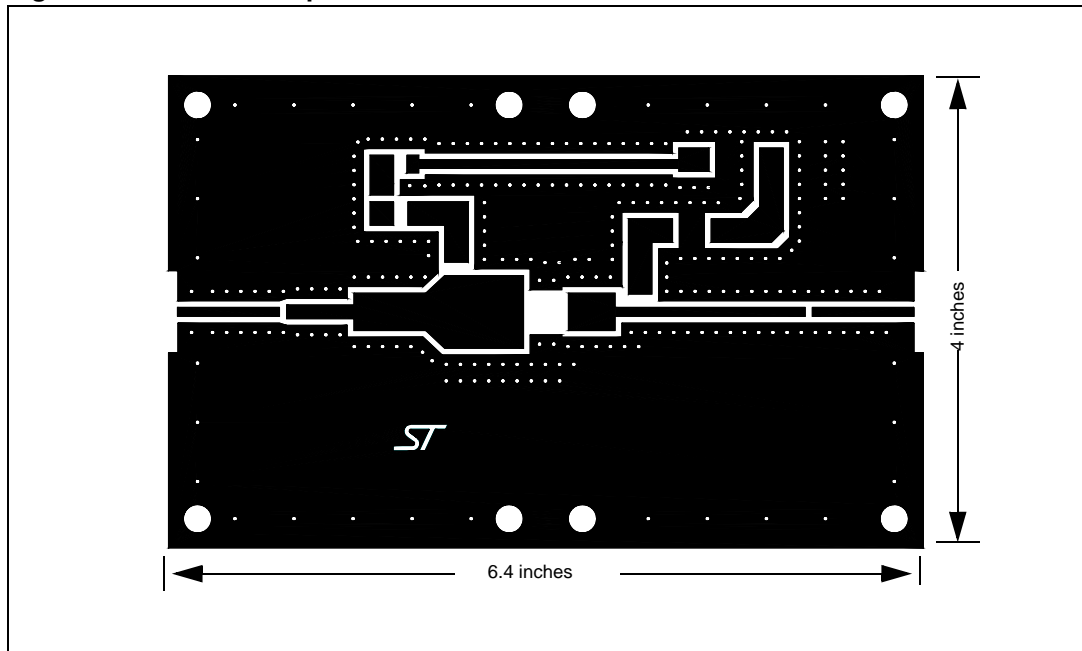
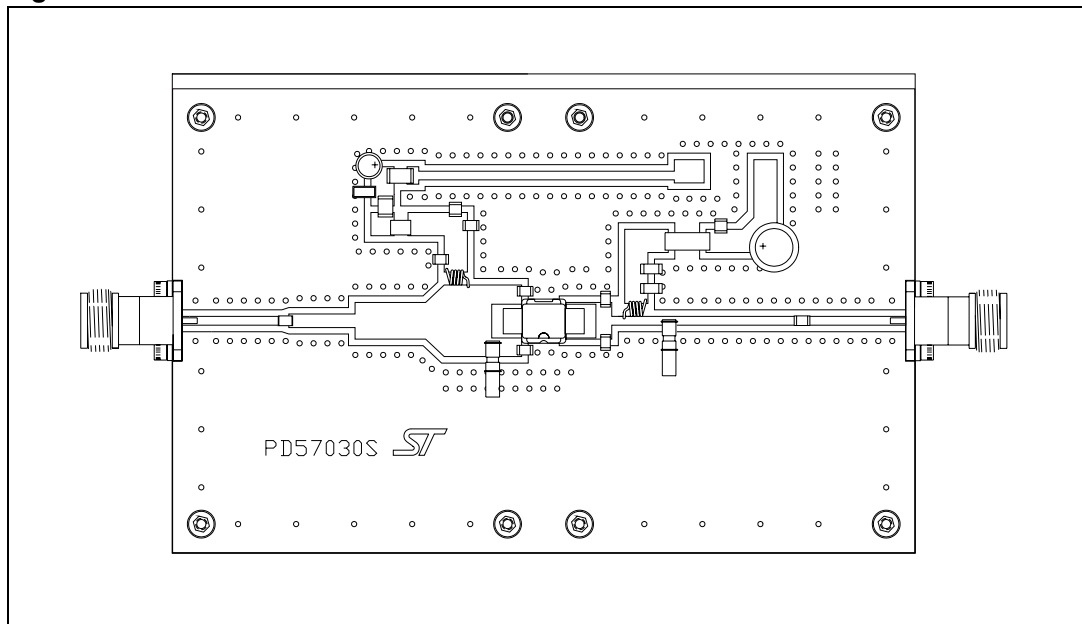


Figure 16. Test circuit



## 6 Package mechanical data

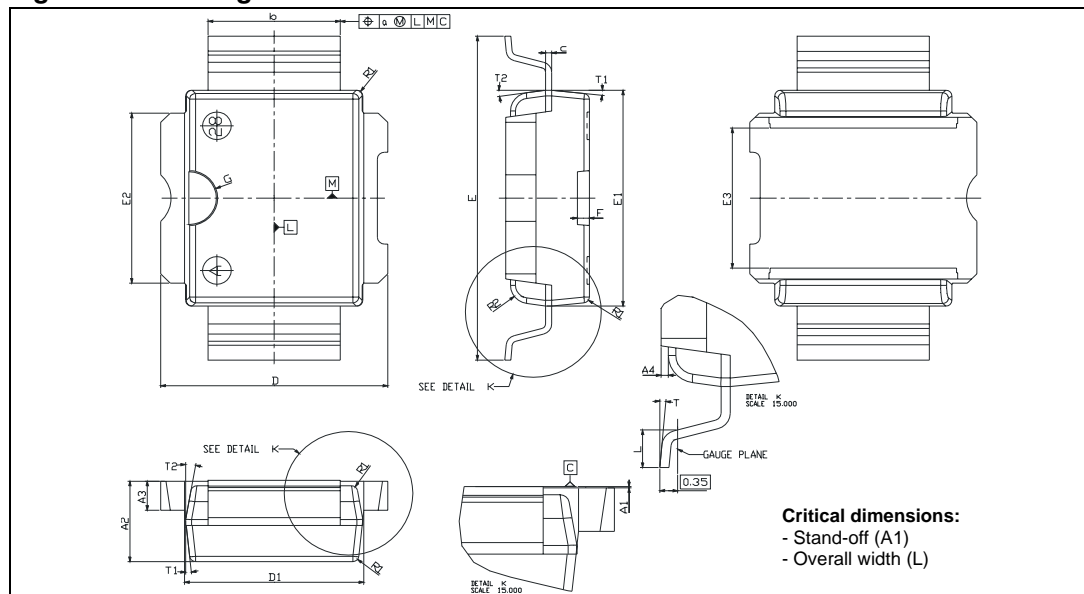
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**Table 7. PowerSO-10RF Formed lead (Gull Wing) Mechanical data**

Dim.	mm.			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1	0	0.05	0.1	0.	0.0019	0.0038
A2	3.4	3.5	3.6	0.134	0.137	0.142
A3	1.2	1.3	1.4	0.046	0.05	0.054
A4	0.15	0.2	0.25	0.005	0.007	0.009
a		0.2			0.007	
b	5.4	5.53	5.65	0.212	0.217	0.221
c	0.23	0.27	0.32	0.008	0.01	0.012
D	9.4	9.5	9.6	0.370	0.374	0.377
D1	7.4	7.5	7.6	0.290	0.295	0.298
E	13.85	14.1	14.35	0.544	0.555	0.565
E1	9.3	9.4	9.5	0.365	0.37	0.375
E2	7.3	7.4	7.5	0.286	0.292	0.294
E3	5.9	6.1	6.3	0.231	0.24	0.247
F		0.5			0.019	
G		1.2			0.047	
L	0.8	1	1.1	0.030	0.039	0.042
R1			0.25			0.01
R2		0.8			0.031	
T	2 deg	5 deg	8 deg	2 deg	5 deg	8 deg
T1		6 deg			6 deg	
T2		10 deg			10 deg	

*Note:* Resin protrusions not included (max value: 0.15 mm per side)

**Figure 17. Package dimensions**



**Table 8. PowerSO-10RF Straight Lead Mechanical data**

Dim.	mm.			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1	1.62	1.67	1.72	0.064	0.065	0.068
A2	3.4	3.5	3.6	0.134	0.137	0.142
A3	1.2	1.3	1.4	0.046	0.05	0.054
A4	0.15	0.2	0.25	0.005	0.007	0.009
a		0.2			0.007	
b	5.4	5.53	5.65	0.212	0.217	0.221
c	0.23	0.27	0.32	0.008	0.01	0.012
D	9.4	9.5	9.6	0.370	0.374	0.377
D1	7.4	7.5	7.6	0.290	0.295	0.298
E	15.15	15.4	15.65	0.595	0.606	0.615
E1	9.3	9.4	9.5	0.365	0.37	0.375
E2	7.3	7.4	7.5	0.286	0.292	0.294
E3	5.9	6.1	6.3	0.231	0.24	0.247
F		0.5			0.019	
G		1.2			0.047	
R1			0.25			0.01
R2		0.8			0.031	
T1		6 deg			6 deg	
T2		10 deg			10 deg	

Note: Resin protrusions not included (max value: 0.15 mm per side)

**Figure 18. Package dimensions**

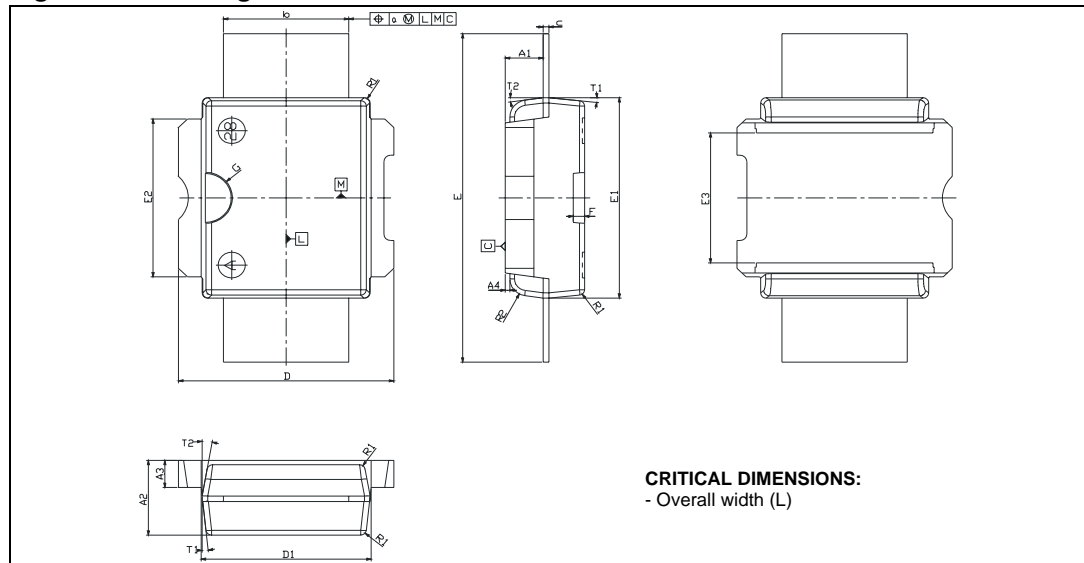
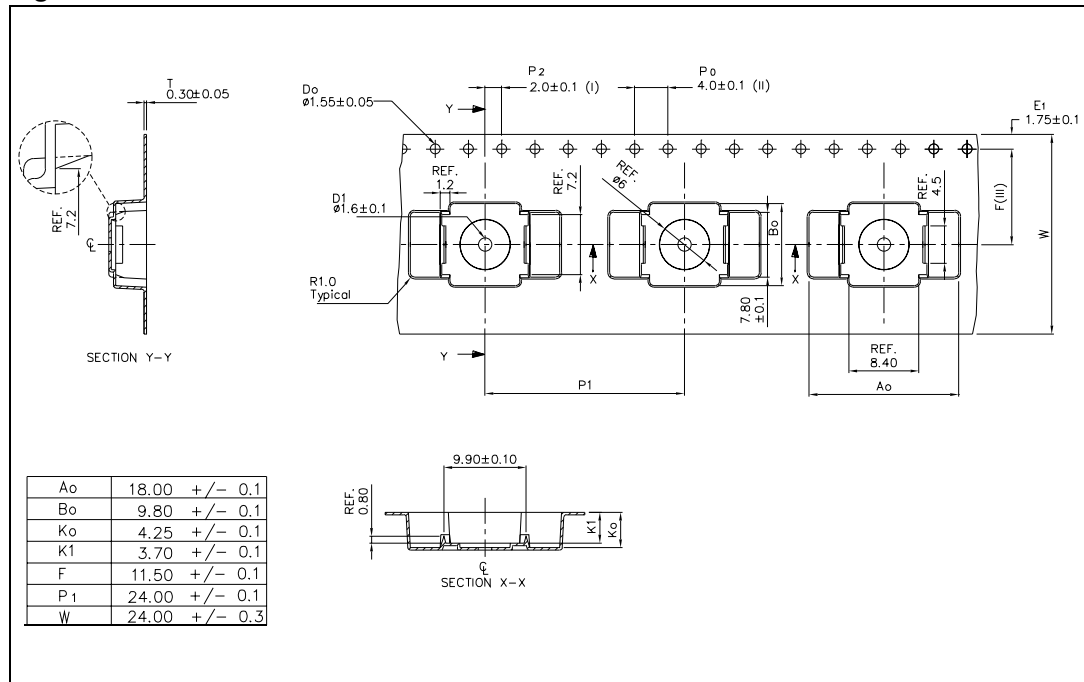




Figure 20. Reel information





## 7 Revision history

**Table 9. Revision history**

Date	Revision	Changes
07-Aug-2006	1	Initial release.

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